Ken-Fu Liang

(+1) 626-265-9085 | kenfuliang@gmail.com | kenfuliang

Summary

A machine learning scientist focuses on the interaction among the fields of deep learning (DL), reinforcement learning (RL), digital signal processing (DSP), graphic processing unit (GPU), and digital integrated circuits (ICs). Optimizing bottom-up from hardware and top-down from algorithm open windows for advanced applications. Ph.D. works focus on brain-computer interfaces (BCIs). Developed a tool to accurately predict the performance of intracortical BCI decoders in closed-loop experiments. This tool, BCI simulator, uses an RNN-based nonlinear neural encoder to closely model kinematic-to-neural relationships and RL-trained nonlinear agents to reproduce natural control policy in monkey experiments. This BCI simulator serves as a platform to help researchers design and develop BCI decoders in simulation, eliminating the need for monkey experiments and saving tons of money and time from building monkey labs. In total, 4 top journal papers (IC, BCI) and 1 conference paper (BCI) and 1 U.S. patent (GPU) have been published.

Education

University of California, Los Angeles (UCLA), Los Angeles, USA *Sep. 2017 - Sep. 2022*

Doctor of Philosophy - PhD, Electrical and Computer Engineering

- Focused on deep learning (DL), reinforcement learning (RL), and brain-computer interfaces (BCI).
- Optimized deep recurrent neural networks (RNN) to closely reproduce neural activity recorded from motor cortex in both single and population levels.
- Quantitatively reproduced control policies by training agents with constrained reinforcement learning.
- Developed accurate and versatile pure-software simulator and real-time physical emulator to predict online performance of BCI decoders.
- Dissertation: Simulation of brain-machine interfaces
- Advisor: Dr. Jonathan Kao
- GPA: 3.88/4.00

National Taiwan University (NTU) , Taipei, Taiwan *Feb. 2012 - Jun. 2013*

Master of Science - MS, Electronics Engineering

- Focused on digital signal processing (DSP), digital IC design, and digital pre-distortion (DPD) techniques for RF IC.
- Thesis: A Quadratic-Interpolated LUT-Based Digital Predistortion Technique for Cellular Power Amplifiers
- Advisor: Dr. Yi-Jan Emery Chen
- GPA: 4.15/4.30

National Chiao Tung University (NCTU), HsinChu, Taiwan *Sep. 2008 - Jan. 2012*

Bachelor of Science - BS, Electrical and Computer Engineering

- Focused on digital signal processing (DSP), mathematics and real-time robotic systems.
- Project: Autonomous Quadrotor.
- Advisor: Dr. Jwu-Sheng Hu
- GPA:3.99/4.00 with 165 credits in 3.5 years

Work Experience

Samsung, California, USA *Nov. 2022 - present*

Engineer

- Design the next generation GPU architecture.

Neuralink, California, USA *Sep. 2022 - Nov. 2022*

Machine Learning Engineer Intern

- Developed algorithm to decode handwriting from intracortical neural signal in real-time.

Meta Platforms, Inc., New York, USA *June 2020 - Sep. 2020*

Research Intern

- Developed algorithm to enable move-and-click cursor control by only decoding forearm EMG signal.

University of California, Los Angeles (UCLA), Los Angeles, USA *Jan. 2019/2020 - Mar. 2019/2020*

Teaching Assistant (Neural Network and Deep Learning)

- Held office hour to teach course material covering machine learning, deep learning, and reinforcement learning for applications including computer vision, natural language processing, and EEG decoding.

MediaTek Inc., HsinChu, Taiwan *Dec. 2013 - Sep. 2017*

Engineer (Parallel Computing Technology division)

- Worked on the first MediaTek mobile GPU chip and Vector Processing Unit for machine learning acceleration and Advanced Driver Assistance System(ADAS).
- Designed and implemented partial GPU hardware and used C/C++ to model GPU hardware behavior for accelerating hardware verification.
- Developed software model for modeling hardware performance and optimizing hardware architecture.

National Taiwan University, Taipei, Taiwan *Aug. 2013 - Nov. 2013*

Full-time research assistant

- Advisor: Prof. Jau-Horng Chen
- Designed digital pre-distortion (DPD) techniques to improve linearity and power consumption for RF IC.

Honors & Awards

May. 2021	**Government Scholarship to Study Abroad**, Supported by Ministry of Education (MOE)	*Taiwan*
July. 2020	**J. Yang Scholarship**, Administered by the Asia Pacific Center (APC).	*UCLA*
Sep. 2018	**University Fellowship**, A rare and high competing fellowship for high performance students.	*UCLA*
Sep. 2017	**Dean's Scholar Award**, A multi-year fellowship for the top entering PhD student awarded by UCLA.	*UCLA*
Sep. 2017	**Living Spring Department Fellowship**, A high competing fellowship for entering PhD student.	*UCLA*
Jun. 2011	**ZyXEL Scholarship**, Awarded to the top junior year student in the ECE, NCTU.	*ZyXEL*
Jan. 2011	**HSIAO YUAN-LUNG ECE Scholarship**, Academic achievement awarded to 2 out of 102 students.	*NCTU*
Jan. 2011	**Academic Achievement Award**, Awarded to the top three students in ECE department.(1st/102)	*NCTU*
Jan. 2010	**Academic Achievement Award**, Awarded to the top three students in ECE department.(1st/102)	*NCTU*
Jan. 2009	**Academic Achievement Award**, Awarded to the top three students in ECE department.(2nd/102)	*NCTU*

Publications & Patents

A closed-loop emulator that accurately predicts brain-machine interface decoder performance
K. F. Liang, J. C. Kao
COSYNE, *Mar. 2022*

An artificial intelligence that increases simulated brain–computer interface performance
S. Olsen, J. Zhang, **K. F. Liang**, M. Lam, U. Riaz, J. C. Kao
IEEE Journal of Neural Eng., *May 2021*

Deep Learning Neural Encoder for Motor Cortex
K. F. Liang, J. C. Kao
IEEE Trans. Bio-Med. Eng., *Nov. 2019*

A wideband Pulse-Modulated polar transmitter usingenvelope correction for LTE applications
K. F. Liang, H. S. Yang, C. W. Chang, and J. H. Chen
IEEE Trans. Microw. Theory Tech., *Aug. 2015*

A Quadratic-Interpolated LUT-Based digital predistortiontechnique for cellular power amplifiers
K. F. Liang, J. H. Chen, and Y. J. E. Chen
IEEE Trans. Circuits Syst. Express Briefs, *Mar. 2014*

Methods of a graphics-processing unit for tile-based rendering of a display area and graphics-processing apparatus,
P. K. Tsung, S. F. Tsai, M. H. Liao, Y. Y. Lin, **K. F. Liang**, and C. S. Liu
US Patent, *Dec. 2016*